Seventh Semester B.E. Degree Examination, Aug./Sept.2020
DSP Algorithms and Architectures

Time: 3 hrs.   Max. Marks:100

Note: *Answer any FIVE full questions, selecting at least TWO questions from each part.*

PART – A

1   a. Explain the two methods of sampling rate conversions used in DSP system, with suitable block diagram and equations. **(06 Marks)**

    b. List and explain the issues that have to be considered while designing and implementing a DSP system. **(04 Marks)**

    c. The sequence $x(n) = [0, 3, 6, 9]$ is interpolated using interpolation sequence $b_K = [\frac{1}{3}, \frac{2}{3}, 1, \frac{2}{3}, \frac{1}{3}]$ and the interpolation factor of 3. Find the interpolation sequence $y(m)$. **(06 Marks)**

    d. Discuss the advantages and disadvantages of FIR filter. **(04 Marks)**

2   a. Explain the circular addressing mode with the help of algorithm. **(06 Marks)**

    b. What is the role of a shifter in DSP? Explain the implementation of 4-bit shift right barrel shifter with a diagram. **(08 Marks)**

    c. Explain the different techniques used to prevent overflow and underflow conditions occurring in MAC unit. **(06 Marks)**

3   a. Draw the functional diagram of the barrel shifter of TMS320C54XX processor and explain its working. **(05 Marks)**

    b. Assume that the current contents of AR3 is 400h, what will be its contents after each of the following TMS320C54XX addressing modes is used? Assume that the contents of AR0 are 40h. (i) *AR3+   (ii) *+AR3(–40h)   (iii) *AR3+0   (iv) *AR3–0B **(04 Marks)**

    c. With an example, explain memory mapped register addressing mode, absolute addressing mode and direct addressing mode. **(06 Marks)**

    d. Explain the PMST register. **(05 Marks)**

4   a. Explain the function of various bits in Timer Control register. **(04 Marks)**

    b. By means of a figure, explain the pipeline operation of the following sequence of TMS320C54XX instructions if the initial value of AR3 is 80 and the values stored in memory location 80, 81, 82 are 1, 2 and 3 respectively.

    LD *AR3+, A
    ADD *AR3+, A
    STL A, *AR3+ **(06 Marks)**

    c. Write an assembly language program of TMS320C54XX processor to compute the sum of three product terms given by the equation, $y(n) = h_0 x(n) + h_1 x(n-1) + h_2 x(n-2)$ using MAC instructions. **(06 Marks)**

    d. Describe the operation of the following instructions of TMS320C54XX processor:
    (i) MPY *AR2–, *AR4+0, B
    (ii) RPT # K **(04 Marks)**

PART – B

5 a. What values are represented by the 16-bit fixed point number N = 4000h in the Q_0, Q_7 and Q_{15} notations? **(06 Marks)**

   b. Write an assembly language for TMS320C54XX processors to multiply two Q_{15} numbers to produce Q_{15} number result. **(06 Marks)**

   c. Write a TMS320C54XX program that illustrates the implementation of an interpolating FIR filter of length 15 and interpolating factor 5. **(08 Marks)**

6 a. Briefly explain scaling and derive the expression for optimum scaling factor for DIT-FFT Butterfly algorithm. **(06 Marks)**

   b. Write the subroutine for bit reverse address generation. Explain the same. **(08 Marks)**

   c. Determine the following for a 512 point FFT computation:
      (i)   Number of stages
      (ii) Number of butterflies in each stage.
      (iii) Number of butterflies needed for the entire computation. **(06 Marks)**

7 a. With a neat schematic diagram, design a data memory system with address range 000800-000FFFh for a C5416 processor. Use 2K × 8 SRAM memory chips. **(06 Marks)**

   b. Draw the I/O interface timing diagram for read-write-read sequence of operation. **(04 Marks)**

   c. Explain the ADC interface in programmed I/O mode. **(06 Marks)**

   d. Explain the context registers required to configure DMA channels. **(04 Marks)**

8 a. With the help of block diagram, explain DSP-based biotelemetry receiver system. **(06 Marks)**

   b. With the help of neat block diagram, explain PCM3002 CODEC. **(06 Marks)**

   c. Explain JPEG encoding and decoding with the help of a block diagram. **(08 Marks)**

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